



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|---------------------|------------------|
| 10/813,599 | 03/31/2004 | Gansha Wu | 42339-198432 | 4361 |
| 26694 | 7590 | 12/07/2006 | EXAMINER | |
| VENABLE LLP P.O. BOX 34385 WASHINGTON, DC 20043-9998 | | | FIEGLE, RYAN PAUL | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2183 | |

DATE MAILED: 12/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|------------------------|---------------------|--|
| Office Action Summary | Application No. | Applicant(s) | |
| | 10/813,599 | WU, GANSHA | |
| | Examiner | Art Unit | |
| | Ryan P. Fiegler | 2183 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 November 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Maintained Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lindwer (US Patent 6,298,434) in view of Raz et al. (Raz) (US Patent 6,606,743).

3. As per claim 1:

A method to execute an instruction on an operand stack, the method comprising:
performing a stack-state-aware translation of the instruction to code to determine an operand stack state for the instruction (Lindwer: column 11, lines 3-22) (the preprocessor moves items from registers to memory and adjusts the SP for the instructions);

dispatching the instruction according to the operand stack state for the instruction (inherent); and

executing the instruction (inherent).

Lindwer does not teach his translation including determining an entry point into shared execution code based on the stack state.

Raz teaches a language accelerator that uses memory-mapped registers as a stack (Raz: column 4, lines 7-12) among other aspects (Raz: column 1, line 60 to column 2, line 10).

Raz's accelerator translates foreign code to native code and uses memory instructions implement the stack operations on the memory-mapped stack (Raz: column 6, lines 33-38).

Thus, the stack state will determine what instructions are used to implement stack operations (e.g. an increment instruction will only pop 1 operand, while an add instruction would pop two, etc.). This, in turn, will affect the overall code length, thus affecting the entry point of the shared code (Raz: column 6, lines 24-51, emphasis on lines 45-51). The examiner is taking the position that the code is shared between the accelerator 34 and the native CPU 16, since both have access to the code.

The code is threaded (Raz: column 4, lines 29-31). The implementation and advantages of multithreading is well known in the art and would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention.

Raz states that his method increases the speed at which Java code is executed (Raz: column 2, lines 11-12). In addition, Raz's method can be readily implemented in any processor (Raz: column 13-19), while Lindwer's cannot.

Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention to implement Lindwer's stack system as in Raz's to be able to execute Java code faster and to be able to implement the method in any processor.

4. As per claim 2:

The method according to claim 1, said performing comprising:

determining a number of operands on the operand stack before the instruction is executed (Lindwer: column 11, lines 3-22) (It is inherent that this step will be taken in moving items from registers to memory and adjusting the SP for the instructions);

determining a number of operands on the operand stack after the instruction is executed based on a number of operands that the instruction consumes and a number of operands that the instruction produces (Lindwer: column 11, lines 3-22); and

inferring a number of shift operations required after execution of the instruction to maintain top-of-stack elements (Lindwer: column 11, lines 3-22).

5. As per claim 3:

The method according to claim 2, wherein the number of shift operations required after execution of the instruction is based on the number of operands on the operand stack before the instruction is executed and the number of operands on the operand stack after the instruction is executed (Lindwer: column 11, lines 15-22).

6. As per claim 4:

The method according to claim 2, wherein the number of shift operations required after execution of the instruction is inferred based on a static lookup table (Lindwer: column 6, lines 39-47) (The translation is based on a static table. Through the table, it is known how many operands will be used and how many will be placed back on the stack, and based on that is how many items are transferred to memory.).

7. As per claim 5:

The method according to claim 1, wherein the operand stack is a mixed-register stack (Lindwer: column 11, lines 15-22).

Art Unit: 2183

8. As per claim 6:

The method according to claim 1, wherein the operand stack state comprises a number of shift operations to maintain top-of-stack elements of the operand stack after the execution of the instruction (Lindwer: column 11, lines 15-22).

9. As per claim 7:

The method according to claim 6, wherein the top-of-stack elements comprise a register stack (Lindwer: column 11, lines 15-22).

10. As per claim 8:

The method according to claim 1, further comprising:
refilling the operand stack (Lindwer: column 11, lines 15-22) (The items are moved based on what will be overwritten, meaning that values pushed on the stack from the routine will refill the register part of the stack.).

11. As per claim 9:

A system comprising:
an operand stack to execute an instruction (Lindwer: column 11, lines 3-5); and
an interpreter to determine a state of the operand stack, translate the instruction into threaded code, and dispatch the instruction based on the state of the operand stack (Lindwer: column 11, lines 3-22) (the preprocessor is the interpreter).

Lindwer does not teach his interpreter determining an entry point into shared execution code based on the stack state.

Raz teaches a language accelerator that uses memory-mapped registers as a stack (Raz: column 4, lines 7-12) among other aspects (Raz: column 1, line 60 to column 2, line 10).

Raz's accelerator translates Java code, in some embodiments, to native code and uses memory instructions implement the stack operations on the memory-mapped stack (Raz: column 6, lines 33-38).

Thus, the stack state will determine what instructions are used to implement stack operations (e.g. an increment instruction will only pop 1 operand, while an add instruction would pop two, etc.). This, in turn, will affect the overall code length, thus affecting the entry point of the shared code (Raz: column 6, lines 24-51, emphasis on lines 45-51). The examiner is taking the position that the code is shared between the accelerator 34 and the native CPU 16, since both have access to the code.

The code is threaded (Raz: column 4, lines 29-31). The implementation and advantages of multithreading is well known in the art and would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention.

Raz states that his method increases the speed at which Java code is executed (Raz: column 2, lines 11-12).

In addition, Raz's method can be readily implemented in any processor (Raz: column 13-19), while Lindwer's cannot.

Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention to implement Lindwer's stack system as in Raz's

Art Unit: 2183

to be able to execute Java code faster and to be able to implement the method in any processor.

12. As per claim 10:

The system according to claim 9, wherein the operand stack is a mixed stack comprising a register stack and a memory stack (Lindwer: column 11, lines 15-22).

13. As per claim 11:

The system according to claim 10, wherein the register stack comprises at least one register to hold at least one respective top element of the stack and the memory stack comprises a contiguous memory region to hold the remaining elements of the operand stack (Lindwer: column 3, lines 15-22).

14. As per claim 12:

A machine accessible medium containing program instructions that, when executed by a processor, cause the processor to perform a series of operations comprising:

translating a virtual machine instruction into threaded code based on an operand stack state of the virtual machine instruction (Lindwer: column 11, lines 3-22);

dispatching the virtual machine instruction according to the operand stack state (inherent); and

executing the instruction (inherent).

Lindwer does not teach his translation including determining an entry point into shared execution code based on the stack state.

Raz teaches a language accelerator that uses memory-mapped registers as a stack (Raz: column 4, lines 7-12) among other aspects (Raz: column 1, line 60 to column 2, line 10).

Raz's accelerator translates Java code, in some embodiments, to native code and uses memory instructions implement the stack operations on the memory-mapped stack (Raz: column 6, lines 33-38).

Thus, the stack state will determine what instructions are used to implement stack operations (e.g. an increment instruction will only pop 1 operand, while an add instruction would pop two, etc.). This, in turn, will affect the overall code length, thus affecting the entry point of the shared code (Raz: column 6, lines 24-51, emphasis on lines 45-51). The examiner is taking the position that the code is shared between the accelerator 34 and the native CPU 16, since both have access to the code.

The code is threaded (Raz: column 4, lines 29-31). The implementation and advantages of multithreading is well known in the art and would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention.

Raz states that his method increases the speed at which Java code is executed (Raz: column 2, lines 11-12).

In addition, Raz's method can be readily implemented in any processor (Raz: column 13-19), while Lindwer's cannot.

Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention to implement Lindwer's stack system as in Raz's

Art Unit: 2183

to be able to execute Java code faster and to be able to implement the method in any processor.

15. As per claim 13:

The machine accessible medium according to claim 12, wherein the threaded code is based on an entry point into shared execution code (Lindwer: column 11, lines 3-22) (it is an entry into a subroutine) (Raz: column 6, lines 45-51).

16. As per claim 14:

The machine accessible medium according to claim 12, further containing program instructions that, when executed by the processor cause the processor to perform further operations comprising:

determining a number of operands that are present on an operand stack at a time before the virtual machine instruction is executed (Lindwer: column 11, lines 3-22) (It is inherent that this step will be taken in moving items from registers to memory and adjusting the SP for the instructions);

determining a number of operands that are present on the operand stack at a time after the virtual machine instruction is executed (Lindwer: column 3, lines 3-22);
and

inferring a number of shift operations required to maintain top-of-stack elements after the virtual machine instruction is executed (Lindwer: column 3, lines 3-22).

17. As per claim 15:

The machine accessible medium according to claim 13, wherein the wherein the number of shift operations required after execution of the instruction is based on the

Art Unit: 2183

number of operands present on the operand stack at a time before the instruction is executed and the number of operands present on the operand stack at a time after the instruction is executed (Lindwer: column 11, lines 15-22).

18. As per claim 16:

The machine accessible medium according to claim 13, wherein the number of shift operations required after execution of the instruction is inferred based on a static lookup table (Lindwer: column 6, lines 39-47) (The translation is based on a static table. Through the table, it is known how many operands will be used and how many will be placed back on the stack, and based on that is how many items are transferred to memory.).

19. As per claim 17:

The machine accessible medium according to claim 12, wherein the operand stack state comprises a number of shift operations to maintain top-of-stack elements of an operand stack after execution of the virtual machine instruction (Lindwer: column 11, lines 15-22).

20. As per claim 18:

The machine accessible medium according to claim 17, wherein the top-of-stack elements comprise a register stack (Lindwer: column 11, lines 15-22).

21. As per claim 19:

The machine accessible medium according to claim 12, further containing program instructions that, when executed by the processor cause the processor to perform further operations comprising:

execute a number of shift operations to replace top-of-stack elements to an operand stack (Lindwer: column 11, lines 15-22) (The items are moved based on what will be overwritten, meaning that values pushed on the stack from the routine will refill the register part of the stack.).

22. As per claim 20:

The machine accessible medium according to claim 19, wherein the number of shift operations is based on a number of elements on the operand stack that are consumed by the virtual machine instruction and a number of elements that are produced by the virtual machine instruction (Lindwer: column 11, lines 15-22) (The items are moved based on what will be overwritten, meaning that values pushed on the stack from the routine will refill the register part of the stack.).

Response to Arguments

23. Applicant's arguments filed 11/6/06 have been fully considered but they are not persuasive.

24. The applicant has made the following argument:

"Raz does not disclose sharing code between the CPU and the language accelerator core. Instead, the language accelerator core is responsive to instructions from the CPU, specifically to memory write commands issued by the CPU to certain specified memory address in the Intelligent Stack."

The language accelerator core generates and places the native code into memory and thus has access to the code. The native CPU has access to the native code as well. Thus, the language accelerator core shares the native code with the

native CPU. This reads on the broadest reasonable interpretation of the term "shared execution code."

Alternatively, Lindwer and Raz could be applied to a multiprocessor system where there are multiple native CPU's. In this case, the code would be shared between the multiple native CPU's.

The point is that, as was pointed out in section 2 of the office action dated 6/22/06 and the personal interview held 7/10/06, the term "shared execution code" is a very broad term. In fact, the examiner understands that the definition of the term that the applicant is actually trying to protect is neither of the definitions offered above. The term "shared execution code" is meant to refer to the reusability of the code segments used to move items in the stack. However, this is only vaguely referred to in paragraph 34 of the specification and the mere mention of avoiding "code duplication" in paragraph 20. **Nowhere** is there an **explicit** definition of the term "shared execution code". It has been discussed that it is the applicant's right to not disclose an explicit definition for such terms, and the examiner understands the applicant's desire to keep the terms as broad as possible; however, it is therefore the examiner's responsibility to apply the broadest reasonable interpretation to the claims.

The claims in fact linger on the verge of being indefinite. Besides the issue with "shared execution code", the term "stack-state-aware translation" is also extremely vague and open to interpretation. Again, the specification offers no **explicit** definition of the term, and besides the small hints throughout the specification, the only suggestion to what the stack state actually refers to is offered in paragraph 30.

The specification as a whole is extremely ambiguous using numerous relative terms (e.g. "may be", "for example", etc.). The abstract is short and uses the same fuzzy language as the claims. The specification lacks a brief summary of the invention. One of ordinary skill of the art would in fact be hard pressed to even comprehend what the invention is trying to accomplish without reading the entire specification, which is sparse on details all together.

Again, this is all within the applicant's right, and the examiner has taken careful consideration to determine that the invention is in fact enabling and definite. However, the claims as presently amended, in conjunction with the present specification, leave a very broad invention that the current references read on.

The following is taken from the MPEP §2106; the most pertinent parts have been bolded:

Claim terms are presumed to have the ordinary and customary meanings attributed to them by those of ordinary skill in the art. *Sunrace Roots Enter. Co. v. SRAM Corp.*, 336 F.3d 1298, 1302, 67 USPQ2d 1438, 1441 (Fed. Cir. 2003); *Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1298, 67 USPQ2d 1132, 1136 (Fed. Cir. 2003) ("In the absence of an express intent to impart a novel meaning to the claim terms, the words are presumed to take on the ordinary and customary meanings attributed to them by those of ordinary skill in the art.") **However, an applicant is entitled to be his or her own lexicographer and may rebut the presumption that claim terms are to be given their ordinary and customary meaning by clearly setting forth a definition of the term that is different from its ordinary and customary meaning.** See *In re Paulsen*, 30 F.3d 1475, 1480, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994) >and *Vitronics Corp. v. Conceptronic Inc.*, 90 F.3d 1576, 1582, 39 USPQ2d 1573, 1576 (Fed. Cir. 1996)<. **Where an explicit definition is provided by the applicant for a term, that definition will control interpretation of the term as it is used in the claim.** *Toro Co. v. White Consolidated Industries Inc.*, 199 F.3d 1295, 1301, 53 USPQ2d 1065, 1069 (Fed. Cir. 1999) (meaning of words used in a claim is not construed in a "lexicographic vacuum, but in the context of the specification and drawings."). Any special meaning assigned to a term "must be sufficiently clear in the specification that any departure from common usage would be so understood by a person of experience in the field of the invention." *Multiform Desiccants Inc. v. Medzam Ltd.*, 133 F.3d 1473, 1477, 45 USPQ2d 1429, 1432 (Fed. Cir. 1998). See also MPEP § 2111.01. If the applicant asserts that a term has a meaning that conflicts with the term's art-accepted meaning, Office personnel should encourage the applicant to amend the claim to better reflect what applicant intends to claim as the invention. If the application becomes a patent, it becomes prior art against subsequent applications. Therefore, it is important for later search purposes to have

the patentee employ commonly accepted terminology, particularly for searching text-searchable databases.

Office personnel must always remember to use the perspective of one of ordinary skill in the art. Claims and disclosures are not to be evaluated in a vacuum. If elements of an invention are well known in the art, the applicant does not have to provide a disclosure that describes those elements. In such a case the elements will be construed as encompassing any and every art-recognized hardware or combination of hardware and software technique for implementing the defined requisite functionalities.

Office personnel are to give claims their broadest reasonable interpretation in light of the supporting disclosure. In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). **Limitations appearing in the specification but not recited in the claim are not read into the claim.** E-Pass Techs., Inc. v. 3Com Corp., 343 F.3d 1364, 1369, 67 USPQ2d 1947, 1950 (Fed. Cir. 2003) (claims must be interpreted "in view of the specification" without importing limitations from the specification into the claims unnecessarily). In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also In re Zletz, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) ("During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow.... The reason is simply that during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed.... An essential purpose of patent examination is to fashion claims that are precise, clear, correct, and unambiguous. Only in this way can uncertainties of claim scope be removed, as much as possible, during the administrative process.").

25. The applicant has made the following argument:

"Raz does not disclose determining an entry point into shared execution code, as there is no shared execution code. There is only one execution code, which is a translation from Java code. This execution code is translated by the language accelerator software and will therefore differ in length from the execution code produced for the same Java code by a different translator, but at no point is the code entered into anywhere but at the very beginning of the code."

The examiner respectfully disagrees. Execution code, especially threaded execution code, is often entered at many different places within the code. A potential entry point is created at each address label produced by a compiler, or, in the case of Lindwer and Raz, the interpreter. Entry points for event handlers used by the program and related programs will need to be determined. Entry points for routines/functions/methods will also need to be determined. Related applications may also use these points. All of the addresses for these address labels for these entry points will rely on the stack state at any one point. The more shifts and moves required

for a particular part of the program, the longer the code, and thus the further in the program subsequent labels will be.

In a very simplistic computing environment where one program is running from beginning to end, yes, there is only one entry point. However, for a complex computing environment at a low level where multiple applications are running indefinitely, simultaneously, switching off, sharing data, and utilizing each other's data assessment tools, the possibilities become much more complicated.

Conclusion

26. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan P. Fiegle whose telephone number is 571-272-5534. The examiner can normally be reached on M-F 8-4:30.

Art Unit: 2183

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ryan P Fiegler
Examiner,
Art Unit 2183


EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100